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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,553	12/29/2003	Rie Tanaka	16869P-010120US	8456

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EXAMINER	
BATAILLE, PIERRE MICHE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,553	TANAKA ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) 1 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is taken in response to Applicant's amendment filed January 31, 2005 responding to Non-Final Action dated September 8, 2004. Applicant's arguments and/or amendments have been considered with the results that follow.

2. Claims 2-21 are pending in the application in prosecution, as Claim 1 has been previously canceled.

Response to Arguments

3. Applicant's arguments with respect to claims 2-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,356,978 (Kobayashi et al) in view of US 5,568,633) Boudon et al.

With respect to claims 2, 12, and 16, Kobayashi teaches a system (Fig. 1) comprising a storage control unit ***(disk control device 11)*** and a plurality of storage

units ***(disk drive device 103)*** for storing data from a host computer ***(host 102)*** wherein the storage control unit includes:

a cache memory (***cache memory 20a, 20b of common memory 12a, 12b)*** for storing data transferred and for storing management information relating to the data stored in the cache memory, and a processor ***(control unit comprising microprocessor 13a, 13b)*** for controlling the storage control unit ***[Col. 4, Lines 54-63]***, the processor having local memory ***(local cache CM 20a, 20b)***, the processor configured to store in its local memory some part of both the data stored in the cache memory and the management information relating to the data stored in the cache memory ***[Col. 4, Lines 41-47; Col. 6, Lines 39-63]***;

the processor storing control program for controlling the storage control unit ***[micro-program such as resource sharing program and area determining program) [Col. 3, Lines 52-58; Col. 4, Line 60 to Col. 5, Line 6]*** the control program configured to operate the microprocessor to process a read request by performing steps of: accessing the local memory to access the in-memory management information; based on the in-memory management information, determining whether read-out data associated with the read request is stored in the cache memory; if the read-out data is stored in the cache memory, then accessing the cache memory to access the read-out data; if the read-out data is not stored in the cache memory, then: accessing the data storage unit to access the read-out data; storing the read-out data in the cache memory; and updating the in-memory management information and the in-cache

management information to indicate an update of the cache memory ***(general principle of cache locality for provided requested data if the data is contained in local cache and if missing the cache, providing the data from external storage, writing back the data in cache and update the management information)*** *[Col. 4, Lines 41-47; Col. 7, Lines 9-51].*

Kobayashi teaches the processor fetches and stores the management information of the cache memory into the memory in the processor ***(Col. 7, Lines 9-16; Col. 7, Lines 32-51)*** the processor updates the management information in the cache memory together with the management information in the processor ***[Col. 4, Lines 41-47; Col. 7, Lines 32-51].***

With respect to claims 2, 12, and 16, Kobayashi fails to teach the local memory and the cache memory storing management information that is used exclusively by at least one microprocessor and exclusive of information used by any other microprocessor. However, Boudon discloses a multiprocessor system carrying the locality functions [Col. 8, Line 62 to Col. 9, Line 23], as required in the claims and as taught by Kobayashi, wherein each processor is associated wit a private cache (3.x, Fig. 1) and a local memory (6.x Fig. 1), and wherein the local memory and the private cache store management information used only by at least one microprocessor. Boudon suggests information initially held in one local memory utilized and modified by one of the processors exclusively with the management processor of the local memory informing or updating the private cache corresponding to the processor that it is the only

memory in possession of the information and that it is not necessary to bring successive modifications back down to the local memory [Col. 10, Lines 56-65].

Therefore, it would have been obvious to one person having ordinary skill in the art, to modify the storage control by Kobayashi and carry the exclusive management features of Boudon as exclusive management would have restricted invalidation of such information by a non-owning microprocessor. Kobayashi suggests the case where, depending on the states of the data bits used, processors are restricted from carry modifications to exclusive information storage in the local memory [Col. 10, Lines 8-65].

With respect to claims 3, 6, 19, Kobayashi additionally teaches identifying vacant or available storage and detecting a fault wherein an area changing means changes a second area into said first area in one of said resource management modules in which a fault is not detected ***[Col. 2, Lines 25-38; Col. 6, Lines 38-61; Col. 12, Lines 43-45]***.

With respect to claims 4-5, 7-11,13-15, 18, and 20-21, Kobayashi teaches: well-known principle of cache memory as cache memory is provided for fast access to local processors while a longer latency period would be required from the same data access in main memory ***[Col. 4, Lines 41-47; Col. 7, Lines 32-51]***; local memory storing some part of data stored and management information for the data stored in the cache wherein the management information includes at least one data attribute for managing the data in the cache memory, a logical address of the data in the cache memory, available storage area information in the cache memory ***[Col. 2, Lines 25-38; Col. 6, Lines 38-61; Col. 12, Lines 43-45]***; the memory in the processor is a volatile memory

[cache memory or common memory with volatile storage, common feature of processor's memory Col. 12, Lines 31-39]; the storage units having a RAID configuration, the storage unit comprising magnetic disks ***[plurality of disk drives with disk configuration being of a known principle of disk array, 103, Fig. 1; Col. 12, Lines 40-45]***.

Conclusion

6. Other prior art made of record and not relied upon, but considered pertinent to applicant's disclosure

US 5,29,442 (Emma) teaching a system provided for management of data in cache memories in a multiprocessor environment which allows portions of lines to be exclusive, while a processor may store into portions of a line under its exclusive control.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on 571-572-4281. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

February 18, 2005

PIERRE BATAILLE
PRIMARY EXAMINER